UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,061	03/29/2001	Richard Louis Arndt	AUS920010117US1	5351

35525 7590 03/29/2004

DUKE W. YEE
CARSTENS, YEE & CAHOON, L.L.P.
P.O. BOX 802334
DALLAS, TX 75380

EXAMINER	
DOOLEY, MATTHEW C	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/821,061	ARNDT ET AL.	
	Examiner	Art Unit	
	Matthew C. Dooley	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05/25/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 49-50 are rejected under 35 U.S.C. 101 because the claimed invention lacks patentable utility. Claims 49 and 50 instructions without structure that fails to provide a tangible process, machine, manufacture, or composition of matter. The claimed material constitutes an arrangement of data bits to be read or outputted, and as such, does not constitute patentable subject matter as required under 35 U.S.C. 101.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is unclear what is being claimed, as it is never demonstrated how to recover the interrupt, let alone what is meant by determining whether the interrupt is recoverable. The specification fails to enable claim 11 and as such, it is rejected.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 11 recites the limitation "the interrupt" in line 3. There is insufficient antecedent basis for this limitation in the claim. Moreover, it is unclear what is being claimed, as it is never demonstrated how to recover the interrupt, let alone what is meant by determining whether the interrupt is recoverable.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1,8,10,12,13,20-22,25-27,30,37,39,41,42,49,50 are rejected under 35 U.S.C. 102(e) as being anticipated by Quach, U.S. 6,625,749.

As per claim 1:

Quach teaches to storing processor information in response to a parity error, determining if the error is recoverable using the stored information, and performing a recovery action if the error is recoverable (Fig.3,4; Col.9: 1-21).

As per claim 8:

Quach teaches to the storage of at least one error state (Fig.3,4; Col.9: 1-21).

As per claim 10:

Quach teaches to saving processor information in response to a error, determining if the error is recoverable using the stored information, and performing a recovery action if the error is recoverable (Fig.3,4; Col.9: 1-21).

As per claim 12:

Quach teaches to the storage of at least one error state (Fig.3,4; Col.9: 1-21).

As per claim 13:

Quach teaches to parity error detection (Col.4: 1-9).

As per claim 20:

Quach teaches to a bus system, a communications unit, a memory including a set of instructions, and a processor that stores processor information in response to a parity error, determining if the error is recoverable using the stored information, and performing a recovery action if the error is recoverable (Fig.1,2a,3,4; Col.9: 1-21).

As per claim 21:

The bus system of Quach is a single bus (Fig.1,2).

As per claim 22:

The system of Quach teaches to primary and secondary bus circuitry (Fig.2a).

As per claim 25:

Quach teaches to a bus system, a communications unit, a memory including a set of instructions, and a processor that stores processor information in response to a parity

error, determining if the error is recoverable using the stored information, and performing a recovery action if the error is recoverable (Fig.1,2a,3,4; Col.9: 1-21).

As per claim 26:

The bus system of Quach is a single bus (Fig.1,2).

As per claim 27:

The system of Quach teaches to primary and secondary bus circuitry (Fig.2a).

As per claim 30:

Claim 30 is the corresponding apparatus claim to method claim 1 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 1.

As per claim 37:

Claim 37 is the corresponding apparatus claim to method claim 8 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 8.

As per claim 39:

Claim 39 is the corresponding apparatus claim to method claim 10 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 10.

As per claim 41:

Claim 41 is the corresponding apparatus claim to method claim 12 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 12.

As per claim 42:

Claim 42 is the corresponding apparatus claim to method claim 13 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 13.

As per claim 49:

Quach teaches to firmware instructions for storing processor information in response to a parity error, determining if the error is recoverable using the stored information, and performing a recovery action if the error is recoverable (Fig.3,4; Col.9: 1-21).

As per claim 50:

Quach teaches to firmware instructions for determining if an error is recoverable, and performing a recovery action if the error is recoverable (Fig.3,4; Col.9: 1-21).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2-7,14-19,31-36,43-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quach, U.S. 6,625,749, in view of Aichelmann, Jr. et al., U.S. 5,659,678.

As per claim 2:

The system of Quach includes error recovery for low level cache systems (Col.4: 1-8). However, it is not taught that an error count should be kept, nor that when the count exceeds a threshold, that the memory cache should be disabled. Aichelmann teaches to a method including keeping an error count, and when the count exceeds a threshold, teaching that the memory cache should be disabled (Fig.4). It would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the error

counting and threshold techniques taught by Aichelmann in the system of Quach because the use of the disabling techniques taught by allows for allocation of defective sectors, and replacement of said sectors to allow for proper operation despite storage errors (Aichelmann: Fig.4; Col.2: 25-31, 58-67).

As per claim 3:

Quach teaches to invalidating look-aside buffer entries (Col.10: 30-40). Moreover, Aichelmann teaches to the use of counting techniques for error logging (Fig.4).

As per claim 4:

Aichelmann teaches to the counting of error types and checking the count against a threshold, and disabling the system if the threshold is exceeded (Fig.4).

As per claim 5:

Aichelmann teaches to real address translation error counting against a threshold, and to the invalidating of the entries (Fig.4; Col.9: 15-61). Moreover, Quach teaches that it is known to invalidate entries inside a look-aside buffer (Col.10: 30-40).

As per claim 6:

Quach teaches to the selected use of entries within the look-aside buffer (Col.10: 40-67).

As per claim 7:

Aichelmann teaches to real address translation error counting against a threshold, and to disabling of the circuitry if the threshold is passed (Fig.4; Col.9: 15-61).

As per claim 14:

The system of Quach includes error recovery for low-level cache systems (Col.4: 1-8). However, it is not taught that an error count should be kept, nor that when the count exceeds a threshold, that the memory cache should be disabled. Aichelmann teaches to a method including keeping an error count, and when the count exceeds a threshold, teaching that the memory cache should be disabled (Fig.4). It would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the error counting and threshold techniques taught by Aichelmann in the system of Quach because the use of the disabling techniques taught by allows for allocation of defective sectors, and replacement of said sectors to allow for proper operation despite storage errors (Aichelmann: Fig.4; Col.2: 25-31, 58-67).

As per claim 15:

Quach teaches to invalidating look-aside buffer entries (Col.10: 30-40). Moreover, Aichelmann teaches to the use of counting techniques for error logging (Fig.4).

As per claim 16:

Aichelmann teaches to the counting of error types and checking the count against a threshold, and disabling the system if the threshold is exceeded (Fig.4).

As per claim 17:

Aichelmann teaches to real address translation error counting against a threshold, and to the invalidating of the entries (Fig.4; Col.9: 15-61). Moreover, Quach teaches that it is known to invalidate entries inside a look-aside buffer (Col.10: 30-40).

As per claim 18:

Quach teaches to the selected use of entries within the look-aside buffer (Col.10: 40-67).

As per claim 19:

Aichelmann teaches to real address translation error counting against a threshold, and to disabling of the circuitry if the threshold is passed (Fig.4; Col.9: 15-61).

As per claim 31:

Claim 31 is the corresponding apparatus claim to method claim 2 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 2.

As per claim 32:

Claim 32 is the corresponding apparatus claim to method claim 3 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 3.

As per claim 33:

Claim 33 is the corresponding apparatus claim to method claim 4 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 4.

As per claim 34:

Claim 34 is the corresponding apparatus claim to method claim 5 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 5.

As per claim 35:

Claim 35 is the corresponding apparatus claim to method claim 6 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 6.

As per claim 36:

Claim 36 is the corresponding apparatus claim to method claim 7 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 7.

As per claim 43:

Claim 43 is the corresponding apparatus claim to method claim 14 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 14.

As per claim 44:

Claim 44 is the corresponding apparatus claim to method claim 15 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 15.

As per claim 45:

Claim 45 is the corresponding apparatus claim to method claim 16 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 16.

As per claim 46:

Claim 46 is the corresponding apparatus claim to method claim 17 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 17.

As per claim 47:

Claim 47 is the corresponding apparatus claim to method claim 18 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 18.

As per claim 48:

Claim 48 is the corresponding apparatus claim to method claim 19 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 19.

11. Claims 9,11,23,28,38,40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quach, U.S. 6,625,749, in view of Moran, U.S. 6,615,374.

As per claim 9:

Quach fails to teach to indicating that a parity error is of a non-recoverable type, when it has been determined as such. Moran teaches to indicating that a parity error is of a non-recoverable type, when it has been determined as such (Fig.2; Col.3: 10-15). It would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the error indication methodology set forth by Moran in conjunction with the system of Quach because the indication allows for specified location error containment and recovery techniques (Moran: 1: 23-27).

As per claim 11:

The system of Moran determines if the interrupt is recoverable (Col.4: 1-20).

As per claim 23:

The system of Moran utilizes a plurality of processors (Fig.1).

As per claim 28:

The system of Moran utilizes a plurality of processors (Fig.1).

As per claim 38:

Claim 38 is the corresponding apparatus claim to method claim 9 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 9.

As per claim 40:

Claim 40 is the corresponding apparatus claim to method claim 11 and as such can is rejected under analogous reasoning to that used above in the rejection of claim 11.

12. Claims 24 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quach, U.S. 6,625,749, in view of Gibson et al., U.S. 6,445,717.

As per claim 24:

It is not precisely shown that the system of Quach is adapted for use in an internet communications system that makes use of a modem and Ethernet adapter. Gibson teaches to the use of parity error recovery systems utilizing modem and Ethernet adapter circuitry in an internet communications system (Col.7: 7-23; Col.13: 30-48). As such, it would have been obvious to make use of the invention of Quach in the system illustrated by Gibson because it allows for a specific environment for the usage of the invention of Quach, namely in an internet system.

As per claim 29:

It is not precisely shown that the system of Quach is adapted for use in an internet communications system that makes use of a modem and Ethernet adapter. Gibson teaches to the use of parity error recovery systems utilizing modem and Ethernet adapter circuitry in an internet communications system (Col.7: 7-23; Col.13: 30-48). As such, it would have been obvious to make use of the invention of Quach in the system illustrated by Gibson because it allows for a specific environment for the usage of the invention of Quach, namely in an internet system.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.	Laberge et al.	U.S. 6,012,148
b.	Dottling et al.	U.S. 6,014,756
c.	Bossen et al.	U.S. 6,332,181
d.	Grochowski et al.	U.S. 6,625,756
e.	Quach et al.	US 2002/0188895

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Dooley whose telephone number is (703) 306-5538. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew Dooley
Examiner AU 2133
3/21/04

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100